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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/981,484	CALLWAY, EDWARD G.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,18-22 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,18,19,21,22 and 29-39* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed October 29, 2007, with respect to Claims 1, 18, and 29-39 are considered but are not persuasive.

2. As per Claim 1, Applicant argues Specification refers to video output ports as connection point with, for example, displays or interfaces for display or are nodes configured as connection node to which a display is coupled that receives video component output and display synchronization information. Office action alleges frame buffer 430 of Normile (US005461679A) is "second video output port", however, frame buffer is not video output port. It is improper to interpret claim to be inconsistent with Applicant's Specification (page 8).

In reply, Examiner understands frame buffer 430 of Normile is not video output port in and of itself. However, frame buffer 430 outputs to display 440 (c. 10, ll. 3-17). So, even though Normile does not explicitly teach "second video output port", there must be video output port connected between frame buffer 430 and display 440 in order for data from frame buffer 430 to be output to display 440. So, Normile is considered to teach second video output port.

3. Applicant argues office action does not address first video component output provides first video output component signal. Office action on one hand alleges video output port is "frame buffer 430" and then on other hand, alleges video output port is "bus". Claim interpretation is inconsistent (page 9).

In reply, Examiner points out Normile discloses "dual-port memory 504 is coupled to control bus 412 for communication between computing module 401 and device over bus 425 such as host 410 and display controller 426" (c. 10, ll. 30-32). Since video processing module

401 (c. 9, ll. 11-15) outputs to bus 425 over bus 412, bus 412 is considered to be first video component output. Since bus 412 outputs from video processing module 401, bus 412 outputs first video output component signal. Bus 425 outputs to display controller 426, and connection between bus 425 and display controller 426 is depicted by line with arrows pointing in opposite directions in Fig. 4. So, even though Normile does not explicitly teach "first video output port", since bus 425 outputs to display controller 426, there must be video output port connected between bus 425 and display controller 426, which is depicted by this connecting line. There must be 2nd video output port connected between frame buffer 430 and display 440 as discussed above, and this is depicted by line connecting frame buffer 430 and display 440 in Fig. 4.

4. Applicant argues that the claim requires that the first video output port is coupled to the first video component output of the graphics device and the first video component output of the second graphics device. The claim would require that bus 420 is coupled to bus 425. Bus 425 of Normile does not provide data to bus 420 nor does bus 420 provide data on the bus 425 (page 9).

In reply, bus 420 outputs to shared memory 405, which outputs to bus 425 (c. 9, ll. 48-58), and so bus 420 provides data on bus 425, and so bus 420 is coupled to bus 425.

5. As per Claim 18, Applicant argues interpretation of Normile for Claim 1 is inconsistent with interpretation taken for Claim 18 which cites to Taylor (US006118461A) since alleged video output ports for which Normile is cited as teaching, would require monitor to be coupled to bus 425 which is not shown in Normile. Normile is coupled to frame buffer 427 or 430 (p. 9-10).

In reply, Normile teaches frame buffers 427, 430 are coupled to monitors 428 and 440, and so bus 425 is still considered to be coupled to monitor 428 (c. 9, ll. 20-24; c. 10, ll. 3-17).

6. As per Claim 29, Applicant argues each device in Walls (US006215486B1) outputs portion of logical frame and not temporally alternating frames or adjacent frames as required. Taylor teaches using subframe system, so, adjacent frame cannot be alternating or temporally adjacent frame of video (pages 10-11).

In reply, Examiner points out Walls is used to teach portion of "logical frame" is entire frame of video (c. 2, ll. 39-41). Taylor is used to teach second portion of frame is output immediately after first portion of frame (c. 6, ll. 50-61; c. 7, ll. 11-30), and this is considered to be temporally adjacent frame of video. Since Taylor is used to modify device of Walls, and since Walls teaches portion of "logical frame" is entire frame of video, device of Walls can be modified so portions of "logical frame" that are entire frames of video are temporally adjacent frames of video, as suggested by Taylor. So, combination of Walls and Taylor teaches this.

7. Applicant argues claims require that 1st graphics device renders entire frame of video and second graphics device renders entire adjacent frame of video. Lengyel (US006016150A) uses 3D pipeline to render single frame by splitting frame into scene layers (p. 12).

In reply, Examiner points out Lengyel is merely used to teach first video output port is coupled to first video component output of first graphics device and to first video component output of second graphics device. This teaching from Lengyel is incorporated into Walls-Taylor combination, which teaches first graphics device renders entire frame of video and second graphics device renders entire adjacent frame of video, as discussed above.

8. Applicant's arguments with respect to claims 19, 21, and 22 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's arguments, see page 10, filed October 29, 2007, with respect to the rejection(s) of claim(s) 19, 21, and 22 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Gonsalves (US006847373B1).

10. As per Claims 19, 21, 22, Applicant argues Deering (US005963200A) teaches attempting to match video sync signals between multiple displays. This is different from attempting to match color component values corresponding to pixel information that is displayed (page 10).

In reply, Examiner agrees. But, new grounds of rejection are made in view of Gonsalves.

Claim Rejections - 35 USC § 103

11. Text of sections of Title 35, U.S. Code 103(a) not included can be found in prior action.

12. Claims 1 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Normile (US005461679A).

13. As per Claim 1, Taylor teaches video driver system having first graphics device (103a, Fig. 1; c. 4, ll. 14-21, 52-57) having input and first video component output to provide first video output component signal; second graphics device (103b) having input and first video component output to provide first video output component signal (c. 4, ll. 50-52; c. 5, ll. 65-c. 6, ll. 1); first video output port (109) coupled to first video component output of first graphics device and first video component output of second graphics device (c. 5, ll. 1-3), as can be seen in Fig. 1.

But, Taylor does not teach 2nd video output port coupled to 1st video component output of 2nd graphics device. But, Normile teaches 1st video device (401, Fig. 4; c. 9, ll. 11-15) having input from host (410, c. 7, ll. 48-49) and 1st video component output (412) to provide first video output component signal (c. 9, ll. 15-17); second video device (402) having input from host (410,

c. 7, ll. 48-49) and first video component output (420) to provide first video output component signal (c. 10, ll. 25-27, 55-57); first video output port (425) coupled to first video component output (412) of first video device (401) (c. 9, ll. 15-17) and first video component output (420) of second video device (402) (c. 9, ll. 48-50; c. 10, ll. 25-27, 55-57); and second video output port (430) coupled to first video component output (420) of second video device (402) (c. 10, ll. 7-11, 25-27, 55-57). Since first video component output 420 of 2nd graphics device 402 outputs video to display 440 (c. 9, ll. 20-24, 48-50; c. 10, ll. 7-19), there must inherently be video output port connected to display 440 in order to output video to display 440. So, there is 2nd video output port coupled to 1st video component output of 2nd video device. Frame buffer 430 outputs to display 440 (c. 10, ll. 3-17). Even though Normile doesn't explicitly teach "second video output port", there must be video output port connected between frame buffer 430 and display 440 in order for data from frame buffer 430 to be output to display 440. Normile discloses "dual-port memory 504 is coupled to control bus 412 for communication between computing module 401 and device over bus 425 such as host 410 and display controller 426" (c. 10, ll. 30-32). Since video processing module 401 (c. 9, ll. 11-15) outputs to bus 425 over bus 412, bus 412 is considered to be first video component output. Since bus 412 outputs from video processing module 401, bus 412 outputs first video output component signal. Bus 425 outputs to display controller 426, and connection between bus 425 and display controller 426 is depicted by line with arrows pointing in opposite directions in Fig. 4. So, even though Normile does not explicitly teach "first video output port", since bus 425 outputs to display controller 426, there must be video output port connected between bus 425 and display controller 426, which is depicted by this connecting line. There must be 2nd video output port connected between frame buffer 430

and display 440 as discussed above, and this is depicted by line connecting frame buffer 430 and display 440 in Fig. 4. Bus 420 outputs to shared memory 405, which outputs to bus 425 (c. 9, ll. 48-58), and so bus 420 provides data on bus 425, and so bus 420 is coupled to bus 425.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Taylor to include second video output port coupled to first video component output of second graphics device because Normile suggests advantage of being able to output to two different displays at the same time (c. 10, ll. 7-19).

14. As per Claim 18, Taylor teaches monitor (110, Fig. 1) coupled to first video output port (c. 5, ll. 1-3). Normile also teaches frame buffers 427, 430 are coupled to monitors 428 and 440, and so bus 425 is coupled to monitor 428 (c. 9, ll. 20-24; c. 10, ll. 3-17).

15. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) in view of Gonsalves (US006847272B1).

Taylor teaches method of providing video signal, method comprising generating first signal at first device (103a, Fig. 1; c. 4, ll. 14-21, 52-57), wherein first signal is representative of first video output component (c. 5, ll. 65-c. 6, ll. 1); providing first signal to first node (109); determining value of first signal at first output node (c. 5, ll. 1-3); generating second signal at second device (103b), wherein second signal is representative of first video output component (c. 4, ll. 52-57); providing second signal of second device to first output node (c. 5, ll. 1-3). Since digital to analog converter receives digital data (first signal) from controller 104 (first output node) and outputs analog data to drive display in response to first signal from first output node (c. 5, ll. 1-3), it must inherently determine value of first signal in order to output analog data,

since it outputs analog data in response to first signal. This means determined value of first signal causes digital to analog converter to output analog data.

But, Taylor does not teach adjusting 2nd device until value of 2nd signal representing color component information at 1st output node substantially matches determined value of 1st signal representing color component data at 1st output node. But, Gonsalves teaches making color modifications to correct color errors due to process errors (c. 1, ll. 26-29). Such corrections include matching colors and tones from shot to shot (c. 1, ll. 34-38). Gonsalves teaches adjusting values of selected destination color component for color matching (c. 3, ll. 42-50; c. 24, ll. 16-19). So, combining Taylor and Gonsalves, it would be obvious to adjust 2nd device until value of 2nd signal representing color component data at 1st output node substantially matches determined value of 1st signal representing color component data at 1st output node.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Taylor to include adjusting 2nd device until a value of 2nd signal representing color component information at first output node substantially matches determined value of first signal representing color component information at first output node because Gonsalves teaches advantage of correcting color errors due to process errors (c. 1, ll. 26-29).

16. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taylor (US006118461A) and Gonsalves (US006847272B1) in view of Deering (US005963200A).

17. As per Claim 21, Taylor and Gonsalves are relied on for teachings relative to Claim 19.

However, Taylor and Gonsalves do not explicitly teach value of 1st and 2nd signals is voltage value. But, Deering teaches adjusting the 2nd device (14) until a value of the 2nd signal at the 1st output node substantially matches the determined value of the 1st signal at the 1st

output node (c. 3, 19-25; c. 5, ll. 22-45), and value of 1st and 2nd signals is voltage value (c. 1, ll. 61-c. 2, ll. 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Taylor and Gonsalves so value of 1st and 2nd signals is voltage value because Deering suggests it is well-known in the art video output is controlled by voltage levels (c. 1, ll. 61-c. 2, ll. 2).

18. As per Claim 22, Taylor does not teach step of determining includes modifying and comparing value of first signal until value of first signal substantially matches predetermined value. However, Deering teaches step of determining includes modifying and comparing value of first signal until value of first signal substantially matches predetermined value (c. 5, ll. 22-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Taylor to include step of determining includes modifying and comparing value of first signal until value of first signal substantially matches predetermined value because Deering suggests advantage that master provides single timing reference (c. 5, ll. 22-45). System utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, because master provides single timing reference, this method avoids exhibiting aberrations in the viewed images.

19. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) in view of Lengyel (US006016150A), further in view of Taylor (US006118461A), further in view of Normile (US005461679A).

Walls teaches multiple graphics devices (202, 204, 206, 208, Fig. 2), each having input (203, 205, 207, 209) and operable to render video for entire screen for one display device that displays portion of complete composite display, such that combination of all of display devices present illusion of one large logical screen that displays complete composite display (c. 1, ll. 28-31, 37-42; c. 2, ll. 19-26, 39-41). Since each graphics device is operable to render video for entire screen for one display device (c. 2, ll. 39-41), each graphics device is considered to render entire frame of video. So, Walls teaches video driver system having first graphics device (202) having input (203) and first video component output to provide first video output component signal; second graphics device (204) having input (205) and first video component output to provide first video output component signal; wherein first graphics device renders entire frame of video, and wherein second graphics device renders entire frame of video.

However, Walls does not explicitly teach first video output port coupled to first video component output of first graphics device and to first video component output of second graphics device. However, Lengyel teaches first graphics device (56, Fig. 2) operative to render first portion (46) of complete composite display (34); and second graphics device (58) operative to render second portion (48) of complete composite display (c. 7, ll. 13-16, 66-67; c. 8, ll. 1-2). Compositor (60) is operatively coupled to receive rendered video (50, 52; c. 8, ll. 30) from any of multiple graphics device and combines input rendered video and outputs it to first video output port (196, Fig. 17) in order to ensure inputs to compositing operation are synchronized (c. 8, ll. 55-60; c. 24, ll. 7-13, 22-27). So, first video output port is coupled to receive rendered video from graphics devices. So, by implementing this compositor taught by Lengyel into device of Walls, device of Walls can be modified so first video output port is coupled to first video

component output of first graphics device and to first video component output of second graphics device; and wherein first graphics device renders video and provides rendered video to first video output port, and wherein second graphics device renders video and provides video to first video output port in order to ensure inputs to compositing operation are synchronized so output of complete composite display is synchronized.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Walls to include first video output port coupled to first video component output of first graphics device and to first video component output of second graphics device because Lengyel suggests advantage of ensuring inputs to compositing operation are synchronized so output of complete composite display is synchronized (c. 24, ll. 7-13, 22-27).

However, Walls and Lengyel do not explicitly teach second graphics device renders temporally adjacent frame of video. However, Taylor teaches frame from frame buffer of display control unit 103a (c. 5, ll. 65-c. 6, ll. 1) is output first to display (110) (c. 6, ll. 50-61), then frame from frame buffer of display control unit 103b (c. 5, ll. 65-c. 6, ll. 1) is output next to display (c. 7, ll. 11-30). Taylor teaches second rendered frame is output immediately after first rendered frame has been output, which is considered to be temporally adjacent frame of video. Taylor is used to modify device of Walls, and since Walls teaches portion of "logical frame" is entire frame of video, device of Walls can be modified so portions of "logical frame" that are entire frames of video are temporally adjacent frames of video, as suggested by Taylor.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Walls and Lengyel so second graphics device renders temporally adjacent frame of video because Taylor suggests since first and second rendered frames are

provided to common port (109; c. 5, ll. 1-3 in Taylor), as is also taught in Lengyel as discussed above, this means only one rendered frame can be output to common port at a time, and so first rendered frame is output first, then second rendered frame is output immediately after first rendered frame has been output (c. 2, ll. 58-c. 3, ll. 15; c. 6, ll. 50-61; c. 7, ll. 11-30), and so first and second rendered frames are adjacent frames of video.

However, Walls, Lengyel, and Taylor do not teach second video output port coupled to first video component output of second graphics device. However, Normile teaches video driver system having first video device (401, Fig. 4, c. 9, ll. 11-15) having input from host (410, c. 7, ll. 48-49) and first video component output (412) to provide first video output component signal (c. 9, ll. 15-24); second video device (402, c. 9, ll. 11-15) having input from host (410, c. 7, ll. 48-49) and first video component output (420) to provide first video output component signal; first video output port (425) coupled to first video component output of first video device and first video component output of second video device (c. 9, ll. 15-24, 48-50; c. 10, ll. 7-19); and second video output port (440) coupled to first video component output of second video device (c. 10, ll. 7-19). This would be obvious for reasons for Claim 1.

20. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) in view of Lengyel (US006016150A).

Walls teaches multiple graphics devices (202, 204, 206, 208, Fig. 2), each operable to render video for entire screen for one display device that displays portion of complete composite display, such that combination of all display devices present illusion of one large logical screen that displays complete composite display (c. 1, ll. 28-31, 37-42; c. 2, ll. 19-26, 39-41). Since each graphics device is operable to render video for entire screen for one display device (c. 2, ll.

39-41), each graphics device is considered to render entire frame of video. So, Walls teaches apparatus for providing video signals having 1st graphics device 202 operative to render entire 1st frame of video; and 2nd graphics device 204 operative to render entire 2nd frame of video.

However, Walls does not explicitly teach common port, operatively coupled to receive first and second frames of rendered video from either of first and second graphics devices. However, Lengyel teaches first graphics device (56, Fig. 2) operative to render first portion (46) of complete composite display (34); and second graphics device (58) operative to render second portion (48) of complete composite display (c. 7, ll. 13-16, 66-67; c. 8, ll. 1-2). Compositor (60) is operatively coupled to receive rendered video (50, 52; c. 8, ll. 30) from any of multiple graphics device and combines input rendered video and outputs it to common port (196, Fig. 17) in order to ensure inputs to compositing operation are synchronized (c. 8, ll. 55-60; c. 24, ll. 7-13, 22-27). So, common port is operatively coupled to receive rendered video from any of the graphics devices. So, by implementing this compositor taught by Lengyel intodevice of Walls, device of Walls can be modified so common port is operatively coupled to receive first and second frames of rendered video from either of first and second graphics devices in order to ensure inputs to compositing operation are synchronized so output of complete composite display is synchronized. This would be obvious for same reasons given in rejection for Claim 29.

21. Claims 31, 38, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) and Lengyel (US006016150A) in view of Taylor (US006118461A).

22. As per Claim 31, Walls and Lengyel are relied upon for teachings relative to Claim 30.

However, Walls and Lengyel do not explicitly teach first frame buffer operatively coupled to first graphics device and second frame buffer operatively coupled to second graphics

device. However, Taylor teaches multiple graphics devices (103, Fig. 1), each operable to render video for portion of complete composite display (c. 4, ll. 14-21, 52-57; c. 5, ll. 65-c. 6, ll. 1). First frame buffer is operatively coupled to first graphics device and second frame buffer is operatively coupled to second graphics device (c. 4, ll. 14-18, c. 4, ll. 19-21).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Walls and Lengyel to include 1st frame buffer operatively coupled to 1st graphics device and 2nd frame buffer operatively coupled to 2nd graphics device because Taylor suggests while images are in process of being drawn and are not yet ready to be displayed, frame buffer can store graphics data defining color/gray-shade of each pixel of entire display frame, so when image is ready to be displayed, pixel data can immediately be retrieved out of frame buffer as corresponding display pixels on display screen are being generated (c. 1, ll. 40-46).

23. As per Claim 38, Walls and Lengyel do not explicitly teach 1st graphics device and 2nd graphics devices are video graphics adapters. However, Taylor teaches first graphics device and second graphics devices (c. 4, ll. 14-18) are video graphics adapters (c. 4, ll. 19-20, c. 4, ll. 49).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Walls and Lengyel so first graphics device and second graphics devices are video graphics adapters because Taylor suggests video graphics adapters are well-known type of graphics device (c. 1, ll. 32-39; c. 4, ll. 46-50). Majority of manufacturers have conformed to VGA graphical standard, making it the lowest common denominator that all PC graphics hardware supports. So, majority of PC graphics hardware would have video graphics adapters, and therefore video graphics adapters are well-known in the art and widely used.

24. As per Claim 39, Walls and Lengyel do not explicitly teach 1st and 2nd rendered frames are adjacent frames of video. But, Taylor teaches frame from frame buffer of display control unit 103a (c. 5, ll. 65-c. 6, ll. 1) is output 1st to display (110) (c. 6, ll. 50-61), then frame from frame buffer of display control unit 103b (c. 5, ll. 65-c. 6, ll. 1) is output next to display (c. 7, ll. 11-30). So, Taylor teaches 1st and 2nd rendered frames are adjacent frames of video. Since Claim 39 does not specify what phrase "adjacent frames of video" means, phrase "adjacent frames of video" is taken to mean that 2nd rendered frame is output immediately after first rendered frame has been output, which is what Taylor teaches. This would be obvious for reasons for Claim 29.

25. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1), Lengyel (US006016150A), and Taylor (US006118461A).
in view of Deering (US005963200A).

Walls, Lengyel, and Taylor are relied upon for teachings discussed relative to Claim 31.

However, Walls does not explicitly teach at least one digital to analog converter operatively coupled to output video. However, Lengyel teaches at least one digital to analog converter (244, Fig. 19) operatively coupled to output video (c. 30, ll. 39-48).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify device of Walls to include at least one digital to analog converter operatively coupled to output video because Lengyel suggests digital to analog converters are well-known in the art (c. 30, ll. 39-48). Video signals from digital source, such as computer, must be converted to analog form if they are to be displayed on an analog monitor, and therefore a digital to analog converter is needed. Digital to analog converters are well-known in the art and widely used.

However, Walls, Lengyel, and Taylor do not teach having voltage adjusted in order to correlate video out voltages being provided by at least one of graphics devices. However, Deering teaches first graphics device (14, Fig. 2) acts as master to second graphics device (14) and adjusting second device until value of second signal at first output node substantially matches determined value of first signal at first output node in order to correlate video out being provided by at least one of graphics devices (c. 3, ll. 19-25; c. 5, ll. 22-45). Deering teaches value of first and second signals is voltage value (c. 1, ll. 61-c. 2, ll. 2). This would be obvious for reasons given for Claims 21 and 22.

26. Claims 33, 34, 36, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) and Lengyel (US006016150A in view of Deering (US005963200A).

27. As per Claim 33, Walls and Lengyel are relied upon for teachings relative to Claim 30.

But, Walls and Lengyel do not teach circuitry operative to provide digital to analog conversion voltage equalization associated with 1st and 2nd graphics devices. But, Deering teaches apparatus for providing video signals having 1st graphics device (14, Fig. 2) operative to render 1st frame of video and 2nd graphics device (14) operative to render 2nd frame of video. Deering teaches circuitry operative to provide digital to analog conversion frequency equalization (c. 5, ll. 12-16). Frequencies produced by RAMDACs will vary within range of values which depends on voltage (c. 4, ll. 57-63). Adjusting frequency means adjusting voltage. This is well-known in the art, and can be found in many publications, such as Wunner (US005095280A) (c. 8, ll. 1-14). So, Deering teaches circuitry operative to provide digital to analog conversion voltage equalization.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify Walls and Lengyel to include circuitry operative to provide digital to analog conversion voltage equalization associated with first and second graphics devices as suggested by Deering because Deering suggests system utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, it is advantageous to include circuitry operative to provide digital to analog conversion frequency or voltage equalization because it avoids exhibiting aberrations in viewed images.

28. As per Claim 34, Walls does not explicitly teach outputting video from second graphics device to common port. However, Lengyel teaches outputting video from second graphics device to common port, as discussed in rejection for Claim 30.

However, Walls and Lengyel do not teach first graphics device includes controller operative to select video from second graphics device to be output. However, Deering teaches master graphics device and slave graphics device (c. 5, ll. 22-25). Master graphics device emits FIELD signal and slave graphics device receives it (c. 5, ll. 25-27). Slave graphics device responds to received FIELD signal by resetting counters which produce video timing signals (c. 5, ll. 30-33). So, Deering teaches first graphics device includes controller operative to select video from second graphics device to be output.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify devices of Walls and Lengyel so first graphics device includes controller operative to select video from second graphics device to be output because Deering suggests this is how master-slave system works (c. 5, ll. 22-33). Deering suggests master-slave system is

advantageous because master provides single timing reference (c. 5, ll. 22-45). System utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, because master provides single timing reference, this method avoids exhibiting aberrations in viewed images.

29. As per Claim 36, Walls and Lengyel do not teach first graphics devices acts as master to second graphics device and provides synchronization control for second graphics device. But, Deering teaches first graphics device (14, Fig. 2) acts as master to second graphics device (14) and provides synchronization control for second graphics device (c. 3, ll. 19-25; c. 5, ll. 22-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify devices of Walls and Lengyel so first graphics devices acts as master to second graphics device and provides synchronization control for second graphics device because Deering suggests advantage that master provides single timing reference (c. 5, ll. 22-45). System utilizing two or more video monitors displaying related or contiguous images generated by two or more computers may exhibit aberrations in viewed images because computers do not operate from single timing reference (c. 3, ll. 12-18). So, because master provides single timing reference, this method avoids exhibiting aberrations in the viewed images.

30. As per Claim 37, Walls and Lengyel do not teach 1st graphics device includes reference signal generator for 2nd graphics controller. But, Deering teaches 1st graphics devices includes reference signal generator for 2nd graphics controller (c. 5, ll. 22-45), as discussed for Claim 36.

31. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walls (US006215486B1) and Lengyel (US006016150A) in view of Eichenberger (see citation below).

Walls and Lengyel are relied upon for teachings as discussed above relative to Claim 30.

However, Walls and Lengyel do not teach load operatively couplable to either one of first and second graphics devices when at least one of the first and second graphics devices is not driving common port. However, Eichenberger teaches use of dummy switch with load coupled to it for charge cancellation of active switch (pp. 257, 260). In other words, the switch that is not active or is not driving the common port acts as the dummy switch and has a load coupled to it.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify devices of Walls and Lengyel to include load operatively couplable to either one of first and second graphics devices when at least one of first and second graphics devices is not driving the common port as suggested by Eichenberger because Eichenberger suggests the advantage of reducing charge injection by charge cancellation (p. 257). The advantages of using dummy switches is well-known in the art and can be found in many publications.

Allowable Subject Matter

32. Claim 20 is objected to as being dependent upon rejected base claim, but would be allowable if rewritten in independent form including limitations of base and intervening claims.

Prior Art of Record

C. Eichenberger, W. Guggenbuhl, "On Charge Injection in Analog MOS Switches and Dummy Switch Compensation Techniques," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 256-264, 1990.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

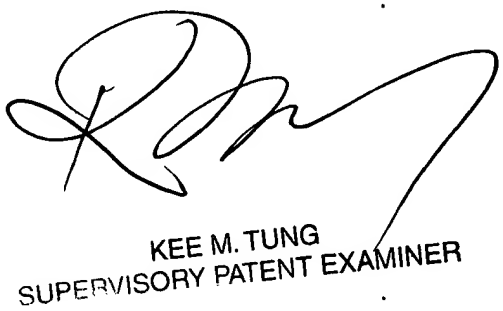
A shortened statutory period for reply to final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on 571-272-7794. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JH



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